Docket No.: SON-3058
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Masaki Murase et al.

Application No.: 10/564,473 Confirmation No.: 9263

Filed: January 13, 2006 Art Unit: 2629

For: DELAY TIME CORRECTION CIRCUIT, VIDEO DATA PROCESSING CIRCUIT, AND FLAT DISPLAY DEVICE Examiner: G. Sitta

APPELLANT'S BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

INTRODUCTORY COMMENTS

This is an Appeal Brief under 37 C.F.R. §41.37 appealing the final decision of the Examiner dated August 20, 2009. Each of the topics required by 37 C.F.R. §41.37 is presented herewith and is labeled appropriately.

This brief is in furtherance of the Final Office Action of August 20, 2009.

A Notice of Appeal was filed in this case on November 19, 2009, along with a Request for Panel Review.

The Notice of Panel Decision from Pre-Appeal Brief Review mailed on January 12, 2010 ("the Decision) indicates that claims 7-22 remain rejected.

The Decision further indicates that the extendable time period for the filing of the Appellant's Brief will be reset to be one month from the mailing of the Decision.

Accordingly, the filing of this Appellant's Brief is timely. 37 C.F.R. §1.136.

I. REAL PARTY IN INTEREST

Sony Corporation of Tokyo, Japan ("Sony") is the real party in interest of the present application. An assignment of all rights in the present application to Sony was executed by the inventor and recorded by the U.S. Patent and Trademark Office at **reel 017481, frame 0587**.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Within the Final Office Action of August 20, 2009:

Paragraph 3 of the Final Office Action indicates a rejection of claims 7-21 as allegedly being unpatentable over the "Background Art" of the specification for the present application (AAPA) in view of Japanese Application Publication No. 2002-009594 (Iemoto).

Paragraph 19 of the Final Office Action indicates a rejection of claim 22 as allegedly being unpatentable over AAPA and Iemoto in view of U.S. Patent No. 6,897,909 (Ochiai).

Thus, the status of the claims is as follows:

Claims 1-6: Canceled

Claims 7-22: Rejected

No claims are indicated within the Final Office Action to contain allowable subject matter.

Accordingly, Appellant hereby appeals the final rejection of claims 7-22 which are presented in the Claims Appendix.

IV. STATUS OF AMENDMENTS

Provided is a statement of the status of any amendment filed subsequent to final rejection.

Subsequent to the final rejection of August 20, 2009, an Amendment After Final Action Under 37 C.F.R. 1.116 has been filed in this case on October 13, 2009.

The Advisory Action dated October 23, 2009 entered of the Amendment of October 13, 2009.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The following description is provided for illustrative purposes and is not intended to limit the scope of the invention.

7. A display device comprising: a level shifter (1) configured to change an amplitude of gradation data (D1) from a first voltage range to a second voltage range, amplified gradation data being said gradation data (D1) at said second voltage range, wherein output data (D2) during a quiescent period (T2) is dummy data (DD), said output data (D2) during a period other than said quiescent period (T2) being said amplified gradation data.	Specification paragraph beginning at page 7, line 20

12. The display device according to claim 10, wherein said quiescent period is a horizontal blanking period.	Specification at page 7, lines 13-19

18. The display device according to claim 15, wherein a horizontal driving circuit converts said resultant gradation data into analog signals.	Specification at page 10, lines 11-18

22. The display device according to claim 15, wherein an active device for processing said resultant gradation data is formed by continuous grain silicon.	Specification at page 21, lines 8-11

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The issues presented for consideration in this appeal are as follows:

Whether the Examiner erred in rejecting claims 7-21 as allegedly being unpatentable over the "Background Art" of the specification for the present application (AAPA) in view of Japanese Application Publication No. 2002-009594 (Iemoto).

Whether the Examiner erred in rejecting claim 22 as allegedly being unpatentable over AAPA and Iemoto in view of U.S. Patent No. 6,897,909 (Ochiai).

These issues will be discussed hereinbelow.

VII. ARGUMENT

In the Final Office Action of August 20, 2009:

The Examiner erred in rejecting claims 7-21 as allegedly being unpatentable over the "Background Art" of the specification for the present application (AAPA) in view of Japanese Application Publication No. 2002-009594 (Iemoto).

The Examiner erred in rejecting claim 22 as allegedly being unpatentable over AAPA and Iemoto in view of U.S. Patent No. 6,897,909 (Ochiai).

For at least the following reasons, Appellant submits that this rejection is both technically and legally unsound and should therefore be reversed.

For purposes of this appeal brief only, and without conceding the teachings of any prior art reference, the claims have been grouped as indicated below.

I. **The Examiner erred in rejecting claims 7-21 as allegedly being unpatentable over the "Background Art" of the specification for the present application (AAPA) in view of Japanese Application Publication No. 2002-009594 (Iemoto).**

A. Claims 7-11, 13-17, 19-21 stand or fall together

Claims 8-11, 13-17, 19-21 are dependent upon claim 7. Claim 7 is drawn to a display device comprising:

> a level shifter (1) configured to change an amplitude of gradation data (D1) from a first voltage range to a second voltage range, amplified gradation data being said gradation data (D1) at said second voltage range,
>
> wherein output data (D2) during a quiescent period (T2) is dummy data (DD), said output data (D2) during a period other than said quiescent period (T2) being said amplified gradation data.

1. AAPA and Iemoto, either individually or as a whole, *fail* to disclose, teach, or suggest a display device wherein *output data during a quiescent period is dummy data*, said output data during a period other than said quiescent period being said amplified gradation data.

a) AAPA

The Final Office Action contends that AAPA discloses the presence of a level shifter (fig. 1 (1)) (Final Office Action at page 2).

However, the Final Office Action ***readily admits*** that AAPA ***fails*** to teach wherein output data during a quiescent period is dummy data (Final Office Action at page 3).

Thus, AAPA fails to disclose, teach, or suggest a display device wherein output data during a quiescent period is dummy data, said output data during a period other than said quiescent period being said amplified gradation data.

b) Iemoto

The Final Office Action cites Iemoto for the features that are admittedly absent from within Iemoto.

Page 2 of the Advisory Action dated October 23, 2009 asserts that Iemoto discloses a delay time stabilizing circuit with dummy pulse generating means in order to reduce fluctuations associated with a delay time.

In response, Figures 1 and 2 of Iemoto are provided hereinbelow.

Figure 1 of Iemoto

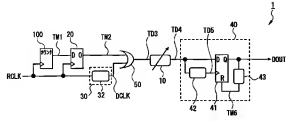
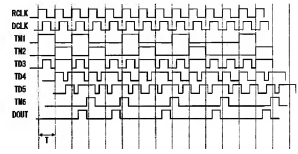


Figure 2 of Iemoto



The machine translation of Iemoto arguably discloses the following at paragraph [0010]:

> [0010]Although *the **vernier 10** is a circuit which acquires a time delay with the variable resolution below a reference signal*, since it has a time delay more than the cycle of a reference signal at least including the fixed delay of a vernier at the time of maximum delay setting out, compared with other logic gates, the delay time variations to a temperature change will become large.

The machine translation of Iemoto arguably discloses the following at paragraphs [0024]-[0026]:

> [0024]The delay circuit 32 is larger than the time delay of the flip-flop 20, and delays the inputted reference signal RCLK within the time of the cycle T and the difference of pulse width of the reference signal RCLK, and *outputs **delay clock signal DCLK to OR gate 50 as a dummy pulse signal***.

[0025]OR gate 50 carries out OR operation of the ***delay clock signal DCLK*** inputted as signal TM2 inputted from the flip-flop 20 from the delay circuit 32, and outputs it to the vernier 10 as ***mix-signals TD3***.

[0026]*The vernier 10 delays* ***mix-signals TD3*** inputted from OR gate 50 according to a preset value by the time resolution below the cycle T of the reference signal RCLK, and *outputs it* to the delay circuit 42 and the flip-flop 41 as *delay pulse signal TD4*.

Claim 7 on appeal provides for amplified gradation data being said gradation data (D1) *at said second voltage range*.

Here, Iemoto ***fails*** to disclose, teach, or suggest ***mix-signals TD3*** as including amplified gradation data.

In this regard, neither the Final Office Action nor the Advisory Action shows where within Iemoto there is disclosed *amplified gradation data being gradation data at a second voltage range*.

As a consequence, *output data during a period other than quiescent period being amplified gradation data* is also ***absent*** from within Iemoto.

Thus, Iemoto fails to disclose, teach, or suggest a display device wherein output data during a quiescent period is dummy data, said output data during a period other than said quiescent period being said amplified gradation data.

c) Combination of AAPA and Iemoto as a whole

The Final Office Action contends that it would have been obvious to one of ordinary skill in the art, at the time of the invention, to incorporate the dummy data during a quiescent period

as taught by Iemoto in order to reduce fluctuations in the operating frequency of the circuit as stated in the abstract of Iemoto (Final Office Action at page 3).

In response, a review of Iemoto reveals an ***absence*** of a level shifter within Figure 1 of Iemoto.

Here, Figure 1 of Iemoto and Figure 1 of AAPA are provided hereinbelow.

Figure 1 of Iemoto

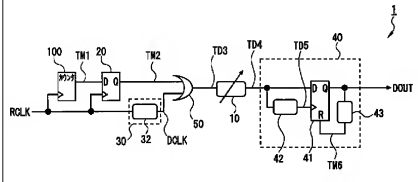
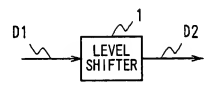


Figure 1 of AAPA



The Advisory Action ***fails*** to show to highlight any disclosure sufficient to show within Iemoto the presence of a level shifter.

Instead, page 2 of the Advisory Action merely asserts that Examiner is *relying on AAPA* to teach the presence of a level shifter (fig. 1 level shifter).

In response, the Final Office Action and the Advisory Action ***fail*** to show where, how and why the skilled artisan would have integrated the level shifter (1) of AAPA into the circuit (1) of Iemoto.

Likewise, the Final Office Action and the Advisory Action ***fail*** to specify the elements within circuit (1) of Iemoto that the level shifter (1) of AAPA is intended to replace. At best, the Final Office Action is incomplete.

Furthermore, page 2 of the Advisory Action asserts that Iemoto teaches a means of inserting dummy data when input data fluctuations associated with logic circuits (CMOS) (abstract), in other words, Examiner is relying on AAPA to teach amplified gradation data.

However, the Final Office Action ***fails*** to show the alleged output data of AAPA and the alleged output data of Iemoto as being one in the same.

Likewise, the Final Office Action and the Advisory Action ***fail*** to specify the output within circuit (1) of Iemoto that the alleged output data of AAPA is intended to replace. Again, the Final Office Action is incomplete.

Regarding AAPA, paragraph [0009] of U.S. Patent Application Publication No. 2006/0164364, the priority document for the present application, provides the presence of a ***period T2***.

However, Iemoto reveals an ***absence*** of a ***time period T2*** within Iemoto.

Moreover, the Final Office Action ***fails*** to show the time periods for the alleged quiescent period of AAPA and the alleged quiescent period of Iemoto as being one in the same.

The Final Office Action attempts an association of the delay clock signal DCLK of Iemoto with the claimed dummy data (Final Office Action at page 3).

Likewise, the Final Office Action apparently attempts an association of the output data D2 of AAPA with the claimed amplified gradation data (Final Office Action at page 2).

In response, Figure 2 of Iemoto and Figure 2 of AAPA are provided hereinbelow.

Figure 2 of Iemoto

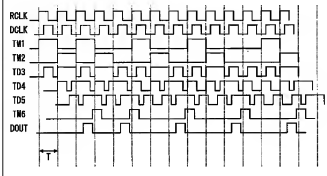
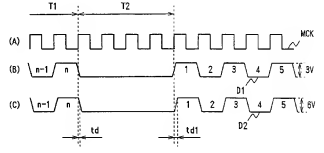


Figure 2 of AAPA



Here, the Final Office Action ***fails*** to show how and why the skilled artisan would have considered any of the mix-signals TD3 of Iemoto as including ***amplified*** gradation data.

Page 2 of the Advisory Action asserts that AAPA discloses all the claimed elements ***except for*** *wherein output data during a quiescent period is dummy data.*

However, the Final Office Action *fails* to show where and how the output data would have been gradation data from AAPA in one instance and any of the mix-signals TD3 from Iemoto in the next instance, especially when there is *no disclosure of time T2 of AAPA within Iemoto*.

B. Claim 12 stands or falls alone

Claim 12 is drawn to the display device according to claim 10, wherein said quiescent period is a horizontal blanking period.

1. AAPA and Iemoto, either individually or as a whole, *fail* to disclose, teach, or suggest a display device wherein said quiescent period is a *horizontal blanking period*.

a) AAPA

Page 4 of the Final Office Action asserts, with emphasis added, that:

> *AAPA **does not disclose** expressly wherein said quiescent period is a horizontal blanking period. However, Applicant has not disclosed that having wherein said quiescent period is a horizontal blanking period instead of a vertical blanking period [0010] provides an advantage, is used for a particular purpose, or solves a stated problem. As such, having quiescent period is a horizontal blanking period is an obvious matter of **design choice**.*

But as shown by the teachings of In re Chu, 36 USPQ2d 1089, 1095 (Fed. Cir. 1995), having quiescent period is a horizontal blanking period would not have been an obvious matter of design choice because:

- The Final Office Action and Advisory Action *fail* to identify a teaching or suggestion in either AAPA or Iemoto that would lead one of ordinary skill in the art to modify Iemoto to place the level shifter (1) of AAPA into the circuit (1) of Iemoto.

The Final Office Action and the Advisory Action *fail* to show the features within claim 12 on appeal are the same as those within AAPA.

Here, a finding of "obvious design choice" precluded where the claimed structure and the function it performs are different from the prior art. In re Chu at 1095 (citing *In re Gal* , 25 USPQ2d 1076 (Fed. Cir. 1992).

As a consequence, the assertion of "obvious design choice" is precluded.

Page 4 of the Final Office Action ***readily admits*** that *AAPA* ***does not disclose*** *expressly wherein said quiescent period is a horizontal blanking period.*

Nevertheless, page 4 of the Final Office Action asserts that: *However, Applicant has not disclosed that having wherein said quiescent period is a horizontal blanking period instead of a vertical blanking period [0010] provides an advantage, is used for a particular purpose, or solves a stated problem.*

In response, the specification for the present application provides the following in the paragraph beginning at page 5, line 16:

> In addition, the present invention is applied to a flat display device so that gradation data is processed by inserting dummy data having a logical level opposite to a logical level during a ***horizontal blanking period*** into the gradation data at a predetermined timing during the ***horizontal blanking period*** of the gradation data.

The specification for the present application provides the following in the paragraph beginning at page 7, line 5:

> Fig. 4 is a block diagram used in explaining a delay time correction principle according to the present invention by contrast with Fig. 1. According to the correction principle, in a data processing circuit for processing input data held at a constant logical level for a constant period at a constant period, dummy data having a logical level opposite to the constant logical level is inserted into the input data at a predetermined timing during a period in which the input level is held at the constant logical level. In addition, the period in which the input data is held at the constant logical level for the constant period at the constant period is a period in which transmission of significant data is not performed, ***such as a horizontal blanking***

period in video data. The period will be hereinafter referred to as the quiescent period as needed.

The specification for the present application provides the following in the paragraph beginning at page 7, line 20:

> More specifically, if the data processing circuit is, for example, a level shifter 1 which, as shown in Fig. 5, corrects input data D1 synchronized with a main clock MCK (Fig. 5(A)) from an amplitude of 0 to 3 (V) to an amplitude of 0 to 6 (V) and outputs output data D2 (Figs. 5(B) and 5(D)), dummy data DD which rises from a logical L level is inserted into the gradation data D1 during a ***horizontal blanking period T2*** in which the gradation data D1 is held at a constant logical level for a constant period at a constant cycle. Accordingly, a reset pulse HDrst based on the dummy data DD is inserted into the gradation data D1 via, for example, an OR circuit 4 (Fig 5(C)).

The specification for the present application provides the following in the paragraph beginning at page 8, line 1:

> Accordingly, according to the correction principle, a delay time dt1 at the rise of the logical level immediately after the ***horizontal blanking period T*** is made short compared to the case where the dummy data DD is not at all inserted, thereby solving the problem that delay time varies according to the length of the immediately preceding logical level. More specifically, if the dummy data DD is inserted in this manner, the logical level of the input data is forcedly switched and the period during which the logical level of the input data is held at a logical L level can be made short compared to the case where the dummy data DD is not at all inserted, so that a variation in delay time can be reduced in a data string of the input data D1. Accordingly, it is possible to effectively avoid latching of erroneous data and the like.

The specification for the present application provides the following in the paragraph beginning at page 8, line 15:

> More specifically, as shown in Fig. 6 by contrast with Fig. 3, in the case where such a logical circuit output is sampled with a subclock SCK (Fig. 6(A)), the dummy data DD is inserted during ***horizontal blanking periods*** in a vertical blanking period VBL, so that the delay time of the output data D2 can be made short at the rise of the logical level following the vertical blanking period VBL and the output data D2 can be sampled and latched at a timing similar to the case of an active video period (Figs. 6(B1) to 6(C2)). Accordingly, it is possible to display a pixel corresponding to the rise of the vertical blanking period VBL with correct gradation. In addition, in the case where black level continues over several lines and rises to white level, or in the case where a particular bit of a plurality of bits rises after being continuously held at an L level over several lines, it is possible to correctly latch the input data D1. Accordingly, a liquid crystal display device can be adapted to correctly display the gradation of each pixel.

The specification for the present application provides the following in the paragraph beginning at page 11, line 22:

> In the processing associated with the gradation data D1, the serial-to-parallel conversion circuit 16 has an OR circuit 27 provided at the output stage of the level shifter 21, and dummy data DD is inserted into the gradation data D1 during the ***horizontal blanking period*** of the gradation data D1 by the OR circuit 27. Accordingly, the liquid crystal display device 11 is adapted to prevent a variation in delay time due to the fact that the gradation data D1 is held at an L level for a long time, so that the gradation data D1 can be correctly latched in the following latch circuits 22 and 23. In addition, the liquid crystal display device 11 is configured to insert the dummy data DD at the output stage of the level shifter 21 in this manner,

because the gradation data D1 is not erroneously latched due to only a variation in delay time occurring in the level shifter 21.

The specification for the present application provides the following in the paragraph beginning at page 12, line 6:

> Accordingly, the timing generator (TG) 14 is configured to output and supply to the OR circuit 27 a reset pulse HDrst by which signal level is risen during each ***horizontal blanking period***.

The specification for the present application provides the following in the paragraph beginning at page 16, line 13:

> For this reason, in this embodiment, as to the gradation data which is input data having a quiescent period during which the input data is held at a constant logical level for a constant period at a constant cycle, the dummy data DD having a logical level opposite to the constant logical level of the gradation data is inserted into the gradation data D1 at a predetermined timing during a ***horizontal blanking period*** which is such quiescent period by the OR circuit 27 provided at the output stage of the level shifter 21. (Figs. 5 and 6).

The specification for the present application provides the following in the paragraph beginning at page 16, line 22:

> Consequently, in the liquid crystal display device 11, as compared with the case where the dummy data DD is not at all inserted, it is possible to eliminate a variation in delay time at the rise of a logical level following a ***horizontal blanking period***, so that it is possible to ensure a delay time similar to the period during which the logical level is inverted at a different duty ratio of 50 (%). Accordingly, this embodiment makes it possible to effectively avoid a variation in delay time in a logical circuit using TFTs or the like. In addition, in a liquid crystal display device which is a data

processing circuit for video data, it is possible to effectively avoid display based on erroneous gradation due to a variation in delay time.

The specification for the present application provides the following in the paragraph beginning at page 18, line 5:

> In addition, in the processing of the gradation data which is video data, by inserting the dummy data DD during each ***horizontal blanking period***, it is possible to correct a variation in delay time and correctly process the video data at the rise of a logical level immediately after a vertical blanking period, and at the rise of a logical level immediately after the logical level falls over a period of several lines.

The specification for the present application provides the following in the paragraph beginning at page 18, line 14:

> The above-mentioned embodiment 1 is configured to insert dummy data during ***a horizontal blanking period*** and prevent an increase in delay time associated with the fall of logical level following the ***horizontal blanking period***, on the basis of the view that it is possible to prevent a variation in delay time in a logical circuit using TFTs or the like by inserting dummy data during a quiescent period.

The specification for the present application provides the following in the paragraph beginning at page 20, line 17:

> In the above description of the embodiments, reference has been made to the case where dummy pulses are inserted during ***horizontal blanking periods***, but the present invention is not limited to this example and dummy pulses may also be inserted during vertical blanking periods as needed.

As a consequence, present within the specification for the present application is a disclosure of the an advantage, a use for a particular purpose, or stated problem solved by "*wherein said quiescent period is a horizontal blanking period instead of a vertical blanking period*".

b) Iemoto

The Final Office Action and the Advisory Action ***fail*** to show within Iemoto a display device wherein said quiescent period is a horizontal blanking period.

C. Claim 18 stands or falls alone

Claim 18 is drawn to the display device according to claim 15, wherein a horizontal driving circuit converts said resultant gradation data into analog signals.

1. AAPA and Iemoto, either individually or as a whole, *fail* to disclose, teach, or suggest a display device wherein a horizontal driving circuit converts said resultant gradation data into *analog signals*.

a) AAPA

Pages 5-6 of the Final Office Action assert that:

> In regards to claim 19, AAPA teaches the display device according to claim 18, wherein a vertical driving circuit sequentially selects pixels through gate lines, said pixels selected through said gate lines being driven by said analog signals [0006].

In response to this assertion, U.S. Patent Application Publication No. 2006/0164364, the publication document for the application on appeal provides the following in paragraph [0006]:

> [0006] Such a liquid crystal display device is configured so as to separate gradation data indicative of gradation of each pixel, which is sequentially inputted in raster scan order, for example, into gradation data for odd lines and even lines and drive the display section based on these gradation data for odd lines and even lines by means of horizontal driving circuits for odd lines and even lines which are respectively provided above and below the display section, so that wiring patterns in the display section are efficiently laid out and the pixels are arranged in fine pattern.

However, ***no analog signal*** is recited within paragraph [0006] of U.S. Patent Application Publication No. 2006/0164364.

b) Iemoto

The Final Office Action and the Advisory Action ***fail*** to show within Iemoto a display device wherein a horizontal driving circuit converts said resultant gradation data into analog signals.

II. The Examiner erred in rejecting claim 22 as allegedly being unpatentable over AAPA and Iemoto in view of U.S. Patent No. 6,897,909 (Ochiai).

A. Claim 22 stands or falls alone

Claim 22 is drawn to the display device according to claim 15, wherein an active device for processing said resultant gradation data is formed by continuous grain silicon.

1. AAPA and Iemoto, either individually or as a whole, *fail* to disclose, teach, or suggest a display device wherein said quiescent period is a *horizontal blanking period*.

Claim 22 is dependent upon claim 7. At least for the reasons provided hereinabove, AAPA and Iemoto, either individually or as a whole, *fail* to disclose, teach, or suggest a display device wherein said quiescent period is a *horizontal blanking period*.

2. Ochiai *fails* to disclose, teach, or suggest a display device wherein said quiescent period is a *horizontal blanking period*.

Ochiai arguably discloses that the term "polysilicon" also encompasses macrocrystalline silicon and ***continuous grain silicon (CGS)*** as well as single-crystal silicon (Ochiai at column 23, lines 48-50).

However, Ochiai is ***silent*** as to the presence of a display device wherein said quiescent period is a *horizontal blanking period*.

III. Conclusion

The claims are considered allowable for the same reasons discussed above, as well as for the additional features they recite.

Reversal of the Examiner's decision is respectfully requested.

If any fee is required or any overpayment made, the Commissioner is hereby authorized to charge the fee or credit the overpayment to Deposit Account # 18-0013.

Dated: February 12, 2010

Respectfully submitted,

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CLAIMS APPENDIX

1-6. (Canceled)

7. (Previously presented) A display device comprising:

a level shifter configured to change an amplitude of gradation data from a first voltage range to a second voltage range, amplified gradation data being said gradation data at said second voltage range,

wherein output data during a quiescent period is dummy data, said output data during a period other than said quiescent period being said amplified gradation data.

8. (Previously presented) The display device according to claim 7, wherein a maximum value of said first voltage range is lower than a maximum value of said second voltage range.

9. (Previously presented) The display device according to claim 7, wherein said first voltage range is 0 volts to 3 volts and said second voltage range is 0 volts to 6 volts.

10. (Previously presented) The display device according to claim 7, wherein said quiescent period is during which said gradation data is held at a constant logical level for a constant period at a constant cycle.

11. (Previously presented) The display device according to claim 10, wherein said dummy data has a logical level opposite to said constant logical level.

12. (Previously presented) The display device according to claim 10, wherein said quiescent period is a horizontal blanking period.

13. (Previously presented) The display device according to claim 10, wherein said quiescent period is a vertical blanking period.

14. (Previously presented) The display device according to claim 10, wherein said gradation data is video data.

15. (Previously presented) The display device according to claim 7, wherein said amplitude of the output data is changed from said second voltage range to said first voltage range, resultant gradation data being said output data at said first voltage range.

16. (Previously presented) The display device according to claim 15, wherein said resultant gradation includes said output data that has been latched on a rising edge of a sampling pulse.

17. (Previously presented) The display device according to claim 16, wherein said resultant gradation includes said output data that has been latched on a falling edge of a sampling pulse.

18. (Previously presented) The display device according to claim 15, wherein a horizontal driving circuit converts said resultant gradation data into analog signals.

19. (Previously presented) The display device according to claim 18, wherein a vertical driving circuit sequentially selects pixels through gate lines, said pixels selected through said gate lines being driven by said analog signals.

20. (Previously presented) The display device according to claim 19, wherein said pixels are arranged in a matrix form.

21. (Previously presented) The display device according to claim 15, wherein an active device for processing said resultant gradation data is formed by low-temperature polysilicon.

22. (Previously presented) The display device according to claim 15, wherein an active device for processing said resultant gradation data is formed by continuous grain silicon.

EVIDENCE APPENDIX

There is no other evidence which will directly affect or have a bearing on the Board's decision in this appeal.

RELATED PROCEEDINGS APPENDIX

There are no other appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.